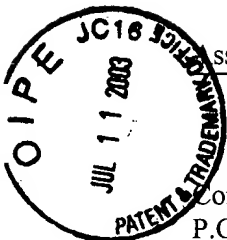


S/N 09/961034

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Madhav Datta et al. Examiner: Long Pham  
Serial No.: 09/961034 Group Art Unit: 2814  
Filed: September 21, 2001 Docket: 884.522US1  
Title: COPPER-CONTAINING C4 BALL-LIMITING METALLURGY STACK FOR  
ENHANCED RELIABILITY OF PACKAGED STRUCTURES AND METHOD OF  
MAKING SAME  
Assignee: Intel Corporation



SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

#9/Suppl.  
IDS  
mR 7/7/03

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Supplemental Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. §1.97(c)(2), Applicants have included the fee of \$180.00 as set forth in 37 C.F.R. §1.17(p). Please charge any additional fees or credit any overpayment to Deposit Account No. 19-0743.

The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

07/14/2003 SSITHIB1 00000073 09961034

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180.00 OP

Respectfully submitted,

MADHAV DATTA ET AL.

By their Representatives,

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Date July 9, 2003

By Ann M. McCrackin  
Ann M. McCrackin  
Reg. No. 42,858

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 9 day of July, 2003

KACIA LEE  
Name

Kacia Lee  
Signature

Substitute for form 1449A/PTO  
**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**  
(Use as many sheets as necessary)



Complete if Known

<b>Application Number</b>	09/961034
<b>Filing Date</b>	September 21, 2001
<b>First Named Inventor</b>	Datta, Madhav
<b>Group Art Unit</b>	2814
<b>Examiner Name</b>	Pham, Long

Sheet 1 of 1

Attorney Docket No: 884.522US1

**US PATENT DOCUMENTS**

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**FOREIGN PATENT DOCUMENTS**

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass
	JP-2001189334	07/10/2001	RI, Soton, et al.	H01L	1/6

**OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS**

Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
		"Chromium Copper Step Phasing", IBM Technical Disclosure Bulletin, (08/01/1977), pgs. 1005-1006
		TUMMALA, RAO, et al., "Microelectronics Packaging Handbook, Semiconductor Packaging", Part 2, 2nd Edition, (1997), pgs. 132-139

**EXAMINER**

**DATE CONSIDERED**